Trends in Microeletronics at the end of Moore's Law

École de microélectronique IN2P3
Frejus - May 18, 2015

A. Marchioro
CERN/PH-ESE

Topics

- Motivation
- Scaling
- Advanced FinFET and other new devices
- Some ideas of advanced circuits, including imagers, from recent major conferences
- Conclusions

Integrated Circuits at the (Energy-Constrained) End of Silicon Scaling

Rob A. Rutenbar

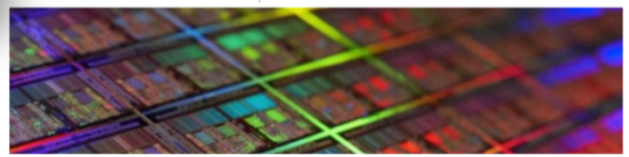
THE END OF CMOS SCALING

TECH

Moore's Law Shows Its Age

Intel's former chief architect: Moore's law will be dead within a decade

By Joel Hruska on August 30, 2013 at 8:30 am | 50 Comments



DARK SILICON AND THE END OF MULTICORE SCALING

Thomas Skotnick
H.-S. Philip Wong

Appears in the Proceedings of the 38th International Symposium on Computer Architecture (ISCA '11)

A KEY QUESTION FOR THE MICROPROCESSOR RESEARCH AND

WHETHER SCALING MULTICORES WILL PROVIDE THE PERFORM

Dark Silicon and the End of Multicore Scaling

Surviving the End of Scaling of Traditional Micro Processors in HPC

Robert G. Clapp
Mencer,

THE END OF DENNARD SCALING

APRIL 15, 2013 ADRIAN MCMENAMIN

The End of Moore's Law?

The current economic boom is likely due to increases in computing speed and decreases in price. Now there are some good reasons to think that the party may be ending.

MYSEMICONDAILY

Semiconductor News and Social Connections

BLOG PHOTOS PARTNERS ABOUT US CONTACT

Posted on July 9, 2014 by sdavis

← Previous Next →

The End of Scaling?

By Jeff Dorsch

Are we reaching the end of scaling?

Yes and no.

TECH 11/13/2011 @ 5:42PM | 1,300 views

The End of Semiconductor Scaling

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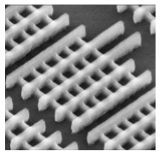


I have repeatedly heard that there is a brick wall facing the world of semiconductors ever since I first worked for National Semiconductor in the late 1970s. Scaling was destined to end, and once it did, the economic force behind the world of semiconductors would come to a grinding halt.

In the early 1980s a co-worker explained to me with conviction that

Replica-of-first-transistor (Photo credit: Revol-web)

What about "More than Moore"

- Until recently CMOS managed to advance to better speed, power and density figures only through the continuous reduction of sizes of devices that could be fabricated reliably.

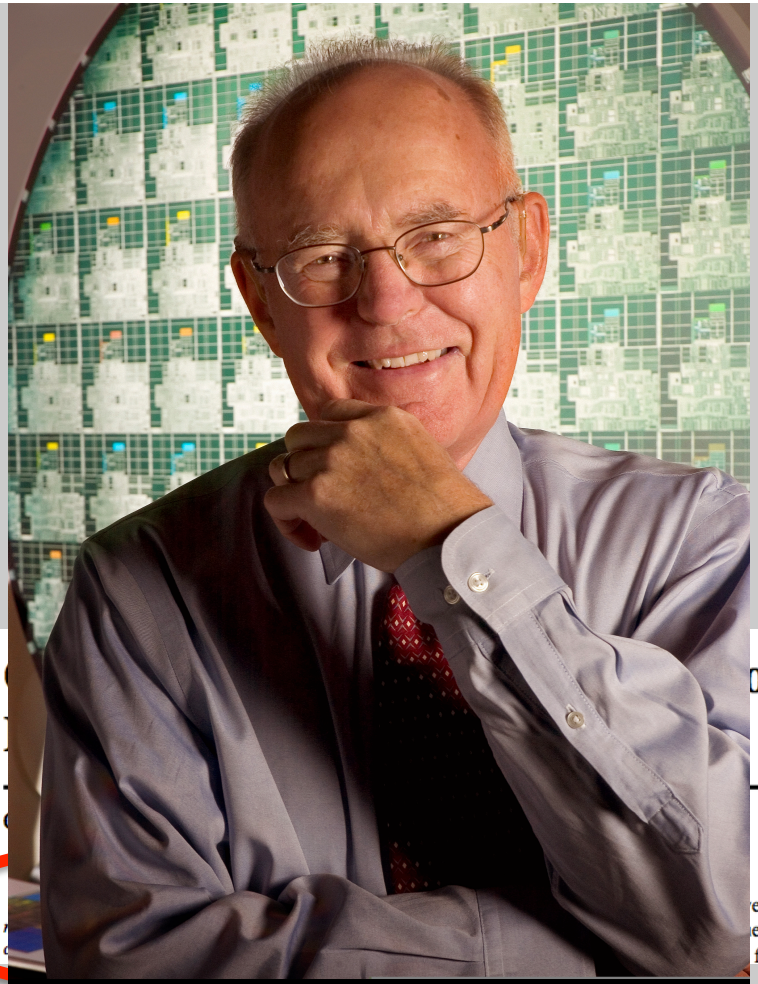
- With the fast approach to hard limits, manufacturers have proposed the continuation of this spectacular growth through a hybridization of the game, i.e. through a new generation of heterogeneous devices that would cover specific needs and application areas (for instance bio-sensors for medical applications, 3D stacking for imagers etc.) with different solutions.

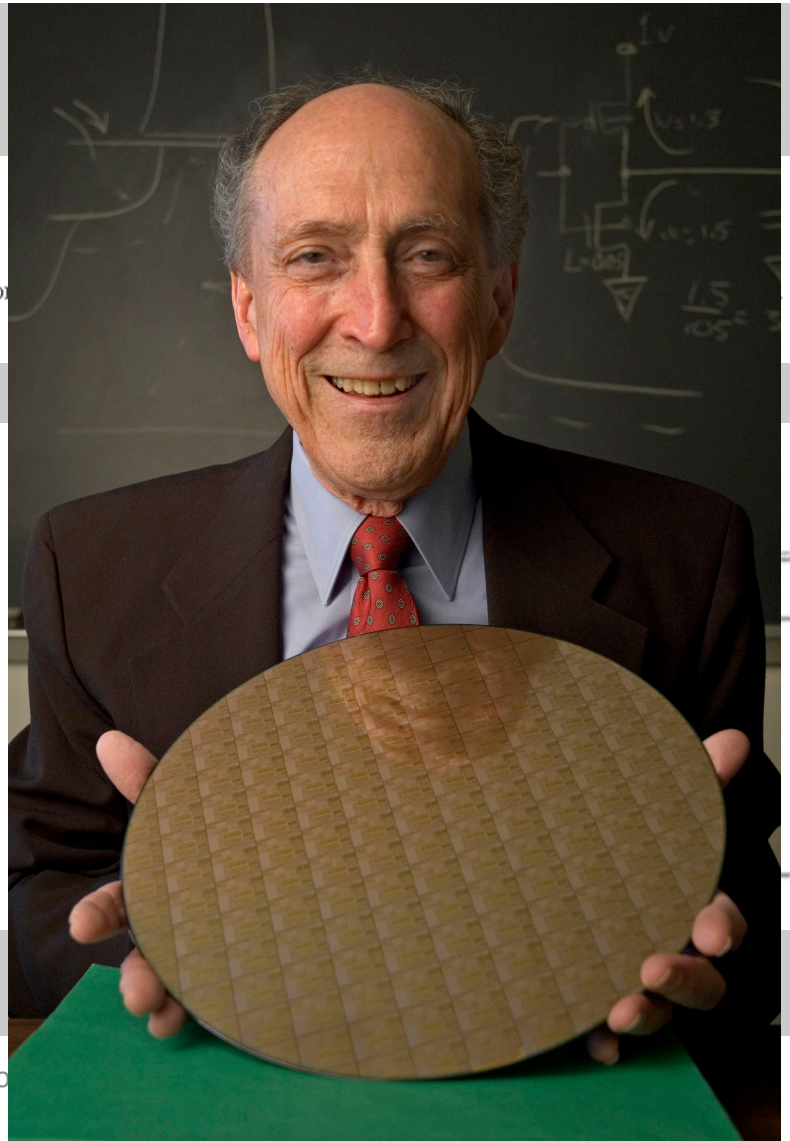
- This model still has to be proven successful, as it violates the basic premise of CMOS development, i.e. "one-technology-fits-all" that worked so well for 40 years.

- On the other side, the M-M model might be beneficial for applications in HEP, if we find a market segment from where to 'borrow' technological advances that can be ported with a *'relatively small'* (financial) effort to our field. For instance, the imagers market could be such a leader to be followed as it is by far the one where the intersection with HEP applications is largest.

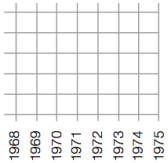
SCALING

Who's scaling





Two gems!



function must be minimized. To do so, we could amortize the engineering over several identical items, or evolve flexible techni[illegible] for the engineering of large functions so that no disproportionate expense need be borne by a particular array. Perhaps newly devised design automation procedures could translate from logic diagram to technological realization without any special engineering.

It may prove to be more economical to build large

Electronics, Volume 38, Number 8, April 19, 1965

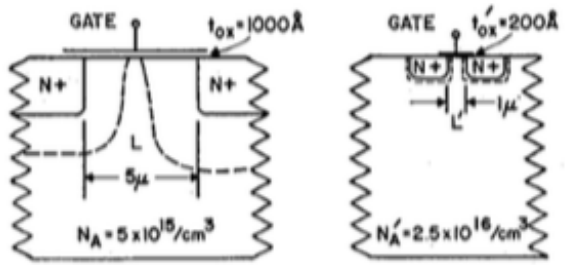
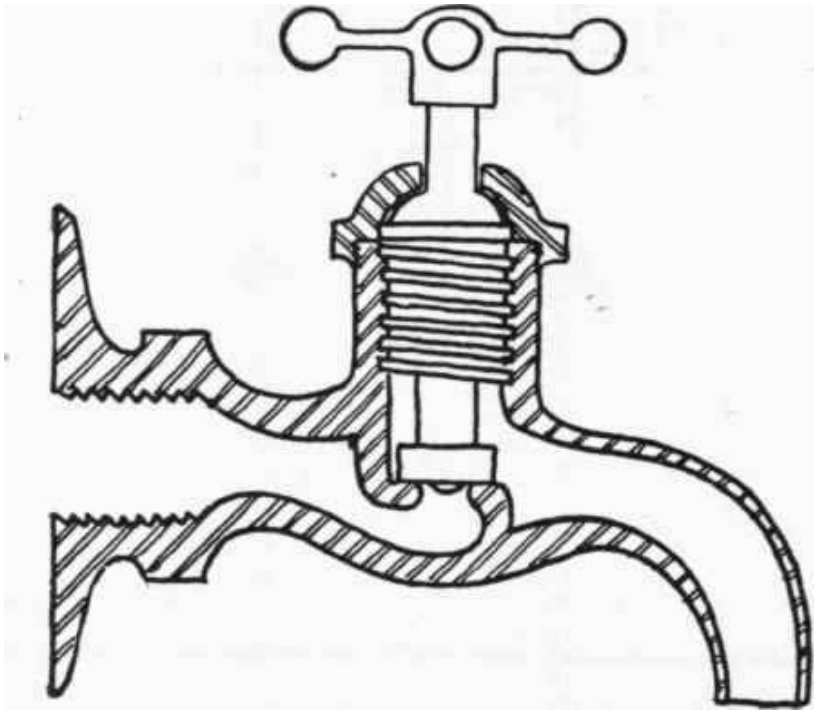


Fig. 1. Illustration of device scaling principles with $\kappa = 5$. (a) Conventional commercially available device structure. (b) Scaled-down device structure.

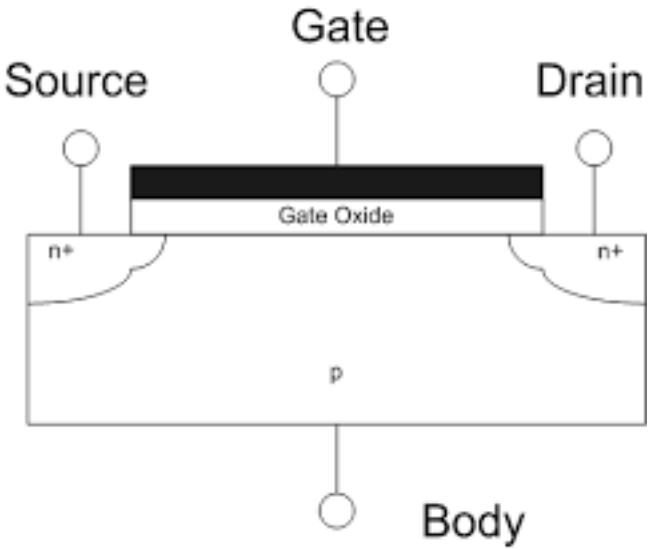
B. Dennard et al.: Design of Ion-Implanted MOSFET'S with Very Small Physical Dimensions

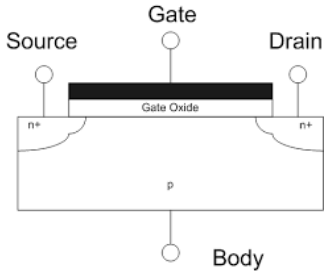
What do we want from a transistor anyway? (sorry engineers…)

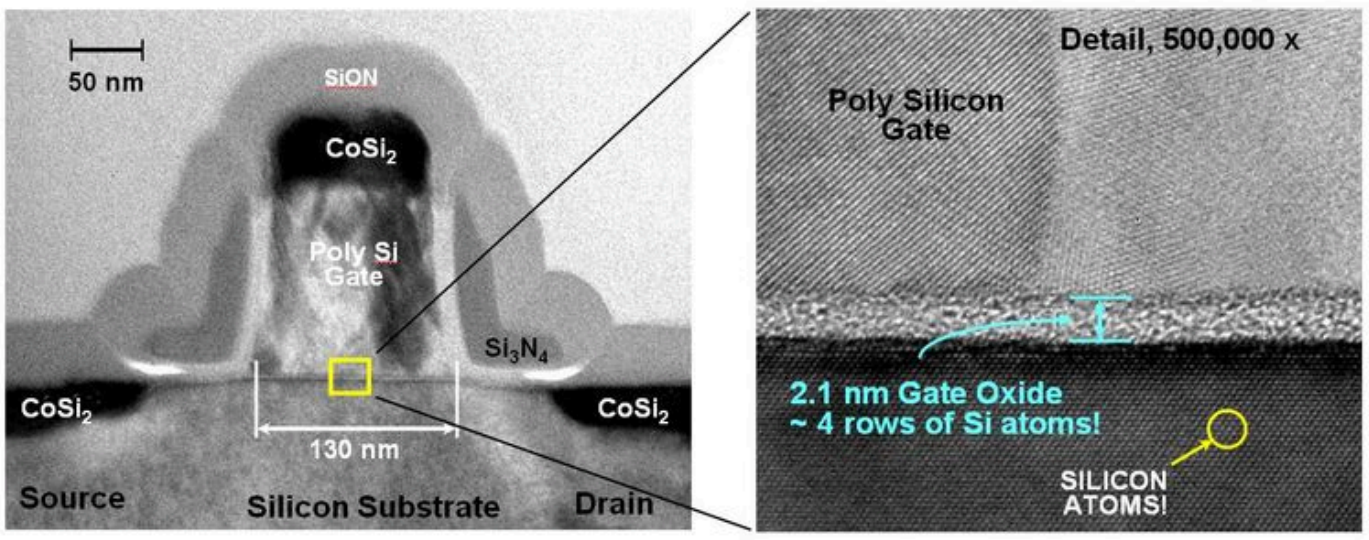
- A transistor (a digital transistor) is a device that has to have the following characteristics:
  - to work as a switch (on or off)
  - make a transition between the two states in a time as short as possible
  - has no leakage current when off
  - has to deliver high current when on (to drive strongly the next stage).
    - Unfortunately this it is not uncorrelated from the previous requirement
  - make a transition between the two states with a voltage drive (Vg) as small as possible
  - control terminal should not be influenced by input/output terminal(s)
  - be physically small (otherwise other “parasitics” ruin the party)
  - Must have complementary type (i.e. a second type which is turned on when the first is turned off using the same “control”).
- Good “analog” characteristics are desirable but by far not necessary or even important for the the majority of technologies being developed.



Scaling of FET



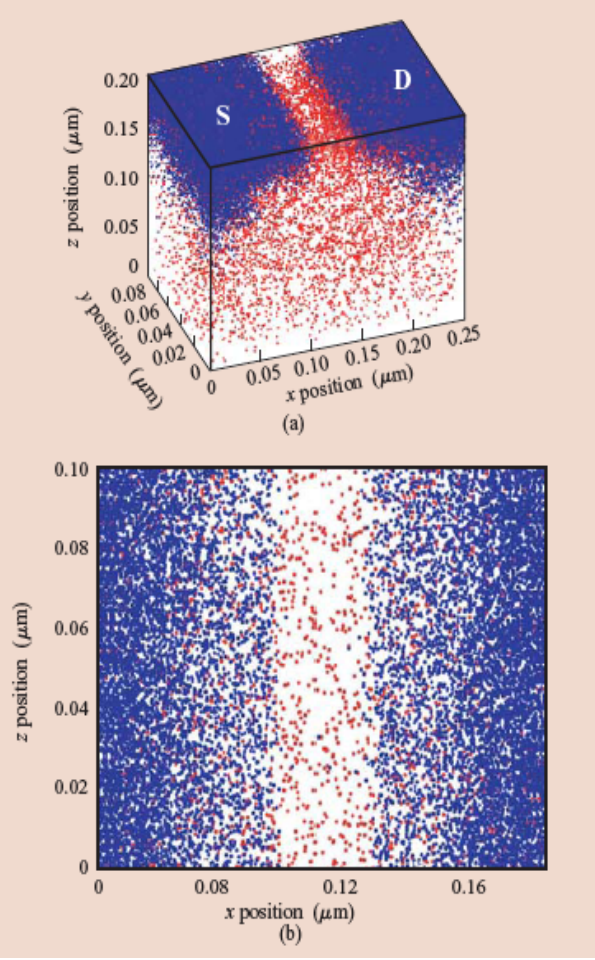




Summary of SC and other effects

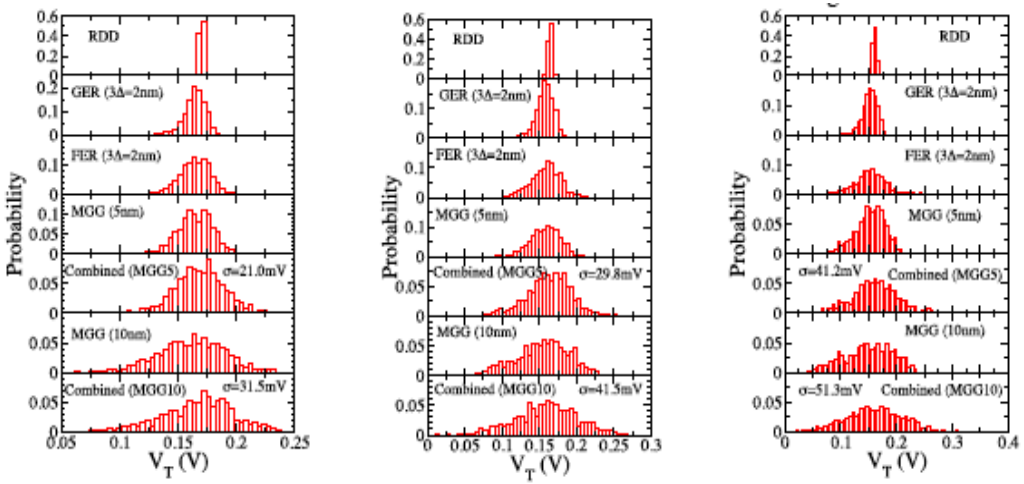
- Drain-to-Source leakage current
- Gate leakage current
- Threshold voltage depends on V_{ds} (DIBL)
- Threshold voltage depends on L
  - SCE and RSCE !
  - Threshold voltage does not stabilize even for large L
- Mobility degradation (vertical electric field too strong)
- Velocity saturation (carriers can't move faster than thermal velocity)
- Poor r_0 and $g_m * r_0$
- Hot electrons
- Punch-through
- Time Dependent Dielectric Breakdown
- …

Atomic Scale Variability



Atomistic view of dopants in 50nm transistor

from K. Bernstein et al.,
IBM J. Res. & Dev. Vol. 50 No. 4/5, 2006



Distribution of Vt on three generations of FinFETS, 20nm, 14nm, 10nm

from X. Wang et al.,
IEDM 2011,

Tricks already in use

TRICKS ALREADY IN USE (APART FROM GEOMETRICAL SHRINKING)		REUSABILITY
– Lithography: many	Print structures << λ	– Sqrt(2)/gen
– High K gate dielectric	*Thicker gate oxide (yes, thicker) to reduce gate leakage*	– ~5x / once
– Strained SiGe channels	*Increase mobility, i.e. faster electrons -> more Ids*	– 25% / once
– Metal gate	*Reduce gate resistance*	– /once
– More metallization layers • *Required complex change in dielectric formation*	*Increase density*	– 1 layer/gen
– Low K inter-metal dielectric	*Reduce cross-capacitance*	– 20%/once, ~few%/gen
– Cu wires	*Reduce interconnect resistance*	– 0.60x / once

What is scaling all about?

- Speed?
  - III-IV materials, Ge
- Low Power?
  - Tunneling effect devices for low ΔV_g switching
- High density?
  - High density multi-chip assembly (many options!)
  - 3D assemblies (wafer on wafer)
  - Fully 3D monolithic ICs (watch what is being done in the area of flash memories!)
- Exotic
  - Ferroelectric memories and resistive RAMs
  - Quantum devices

	Speed	Power	Density
CMOS (until recently)	☺	☺	☺
III-V or Ge	☺	☹	😐
New devices with enhanced Sub Slope	☺	😐	😐
3D	☺	☹	☺
Quantum	?	?	??

Scaling and Interconnects

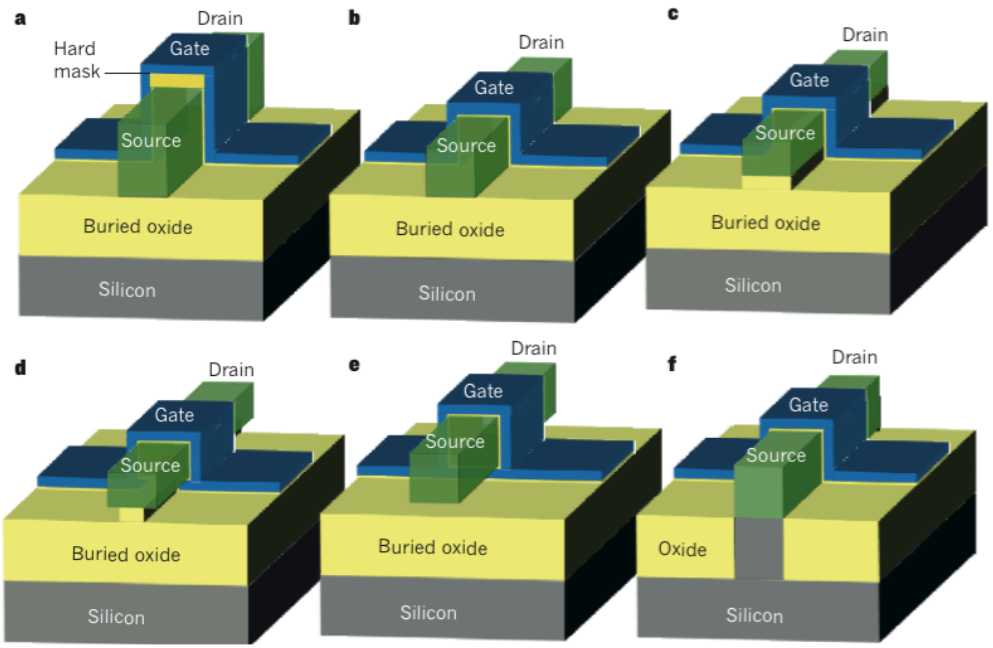
	2015	2020
Technology generation: gate length [nm]	17	11
M1 Metal Pitch for logic [nm]	42	24
Gate density: 4-NAND/mm2	4 E6	1 E7
Max number of metals	13	14
Capacitance per unit length [pF/cm]	1.8-2	1.6-1.8
Intrinsic FinFET NMOS delay (=CV/I) [ps]	.32	.19
NMOS Power indicator [fJ/um]	.42	.25
$ # M1 Cu line R per um [Ω/um]	100	400
$ Distributed RC delay per mm M1 wire (=0.4*r*c(L^2)) [ns]	7.6	29
$ Length at which $\tau_{int} = \tau_{wire}$ [um]	6.5	2.5

from ITRS 2012, 2012U and 2013 editions
$: computed value
: do not use the "standard" value for Cu resistivity, this is much higher for very thin wires where size of metal grains is comparable with thickness

MOORE'S++
FINFET AND GATE CONTROL

Multi-gate devices

- Intel Tri-gate
- TSMC, Samsung and GF Finfets
- STM FDSOI



from: Ferain, **"Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors "**,

Quiz

- Who invented the FinFET ?

1. Mighty Intel
2. IBM Yorktown
3. A University Professor
4. A Korean Research Institute

This guy (partially)

Prof. Chenming Hu
UC Berkeley

is the silicon substrate. So you really have to do something on both sides so you're pinching against something firm, and that's what the FinFET is doing. We should pinch the channel [where electrons flow] on two sides and on top. The more pinching sides, the better.

Pinching the hose will allow us to use a much, much shorter hose. That's extremely important. Making things small is really the key of making the electronics cheaper, faster, and lower power.

IEEE Spectrum: The idea for FinFETs has been around for a while. How did it all get started?

Chenming Hu: DARPA [the Defense Advanced Research Projects Agency] sent out a request for proposals in 1996 for ideas to develop electronic switches beyond 25 nm. At the time, the industry was using 250-nm transistors, and the general view was that transistors could not be scaled below 100 nm. But my students and I had already been thinking about how to get transistors to scale to 25 nm and beyond.

There was a quick meeting probably lasting only five minutes between myself and two colleagues—Professor Tsu-Jae King Liu and Professor Jeff Bokor. The meeting was short because we already knew what to do.

I was on a flight to a conference in Japan, and I had about 10 hours, so I just wrote down the technical proposal in longhand. I proposed two structures that we'd been thinking about for a while. One was FinFETs, and the other is what we call an ultrathin-body silicon-on-insulator (UTB SOI).

We got the contract in 1997, and that gave us the resources to demonstrate FinFETs experimentally. A young graduate student named Xuejue "Cathy" Huang made the working device, and the team of three professors and 11 students and visiting researchers published it in 1999.

This proves that long flights are useful!

First Berkeley FinFET Paper

Sub 50-nm FinFET: PMOS

Xuejue Huang, Wen-Chin Lee, Charles Kuo, Digh Hisamoto*, Leland Chang, Jakub Kedzierski, Erik Anderson**, Hideki Takeuchi, Yang-Kyu Choi, Kazuya Asano^, Vivek Subramanian, Tsu-Jae King, Jeffrey Bokor and Chenming Hu

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^NKK Corp., Japan

Abstract

High performance PMOSFETs with gate length as short as 18-nm are reported. A self-aligned double-gate MOSFET structure (FinFET) is used to suppress the short channel effect. 45 nm gate-length PMOS FinFET has an I_{dsat} of 410 μA/μm (or 820 μA/μm depending on the definition of the width of a double-gate device) at Vd = Vg = 1.2 V and Tox = 2.5 nm. The quasi-planar nature of this variant of the double-gate MOSFETs makes device fabrication relatively easy using the conventional planar MOSFET process technologies. Simulation shows possible scaling to 10–nm gate length.

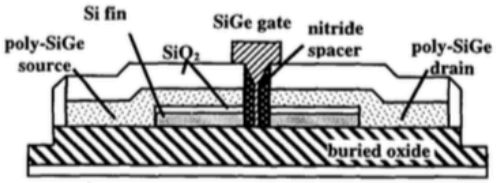


Figure 1: Schematic drawing of FinFET

Fig. 1 shows an exploded view of the FinFET device. The following process sequence was used to fabricate the device. 100 nm SOI film over buried oxide was thinned to 50 nm by thermal oxidation. Ion implantation established a body

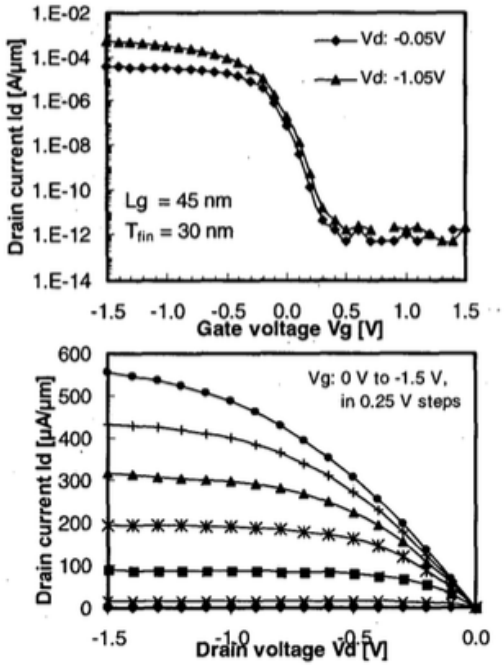


Figure 6: IV characteristics for 45-nm gate length and 30-nm thick Si body PMOS device

Published in:
Electron Devices Meeting, 1999. IEDM '99. Technical Digest. International

More complete LBL FinFET Paper

FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm

Digh Hisamoto, *Member, IEEE*, Wen-Chin Lee, Jakub Kedzierski, Hideki Takeuchi, Kazuya Asano, *Member, IEEE*, Charles Kuo, Erik Anderson, Tsu-Jae King, Jeffrey Bokor, *Fellow, IEEE*, and Chenming Hu, *Fellow, IEEE*

***Abstract*—MOSFETs with gate length down to 17 nm are reported. To suppress the short channel effect, a novel self-aligned double-gate MOSFET, FinFET, is proposed. By using boron-doped $Si_{0.4}Ge_{0.6}$ as a gate material, the desired threshold voltage was achieved for the ultrathin body device. The quasiplanar nature of this new variant of the vertical double-gate MOSFETs can be fabricated relatively easily using the conventional planar MOSFET process technologies.**

***Index Terms*—Fully depleted SOI, MOSFET, poly SiGe, short-channel effect.**

I. Introduction

TO DEVELOP sub-50-nm MOSFETs, the double-gate structure has been widely studied. This is because

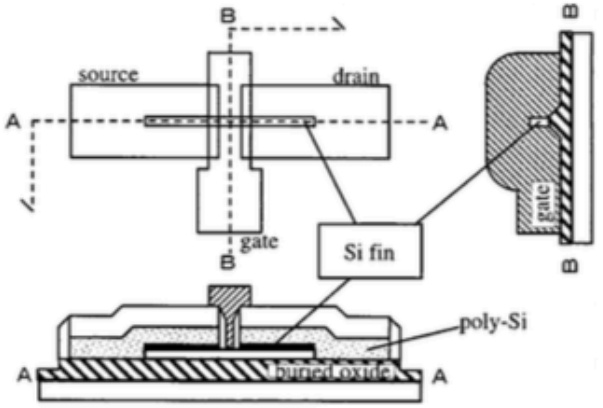


Fig. 1. FinFET typical layout and schematic cross sectional structures.

quasi planar technology. In this paper, the fabrication process and the device characteristics in the sub-50 nm gate-length region are presented. We demonstrate the feasibility of the new device structure named FinFET.

Previous ideas

Monte Carlo Simulation of a 30 nm Dual-Gate MOSFET: How Short Can Si Go?

D. J. Frank, S. E. Laux and M. V. Fischetti

IBM Research Division, T. J. Watson Research Center
P.O. Box 218, Yorktown Heights, NY 10598

Conclusions

In summary, it appears that high performance Si MOSFETs can be scaled down to gate lengths of order 30 nm. Such devices are still suitable for digital circuitry, and may have transconductances as high as 2300 mS/mm and ring oscillator speeds near 1 ps. The technology needed to do this includes thickness control of very thin layers, dual gate alignment, very abrupt doping profiles and gate work function control. A high thermal conductivity method of removing heat from such devices would also need to be found.

References

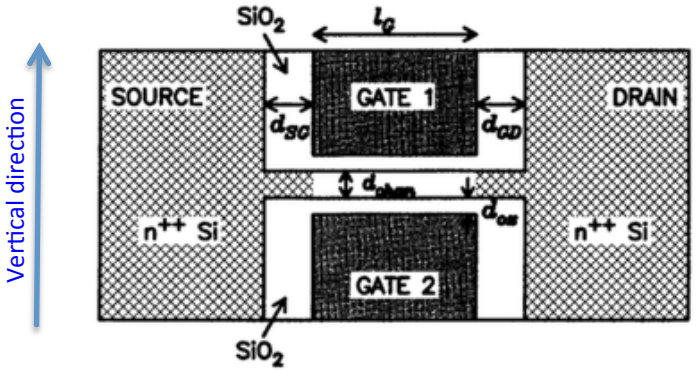


Fig. 1. Dual-gate MOSFET cross-section. Our simulations all use $d_{ox} = 3$ nm, $d_{SG} = d_{GD} = 0.3 \times l_G$, and 10^{20} cm^{-3} n-type source and drain doping.

Previous ideas++

Design and Performance Considerations for Sub-0.1μm Double-Gate SOI MOSFET's

Hon-Sum Wong, David J. Frank, Yuan Taur, and Johannes M.C. Stork[1]

I.B.M. Thomas J. Watson Research Center,
P.O. Box 218, Yorktown Heights, New York 10598, U.S.A.

ABSTRACT

We present a simulation-based analysis of the device design and circuit performance trade-offs between short channel immunity and parasitic device capacitances of sub-0.1μm double-gate SOI MOSFET's. We demonstrate that perfect alignment of the bottom gate to the top gate is not necessary to achieve adequate short channel immunity but is required to maintain short gate delays. Double-gate MOSFET device design guidelines are provided.

in reduced worst-case short-channel immunity and lower current drive for MBG due to the weaker backgate control when the bottom gate is offset from the drain (Fig. 1(d)) or the source (Fig. 1(e)).

DEVICE DESIGN

source/drain doping (Fig. 1(a)). However, fabrication of DG-SOI at the 100 nm regime with this ideal self-aligned structure is difficult. A promising approach presented recently [5] is the "flip-bonded-etchback SOI" method in which the bottom gate is formed prior to the bonded-etchback process and the subsequent formation of the top gate and source/drain structures. In this method, the bot-

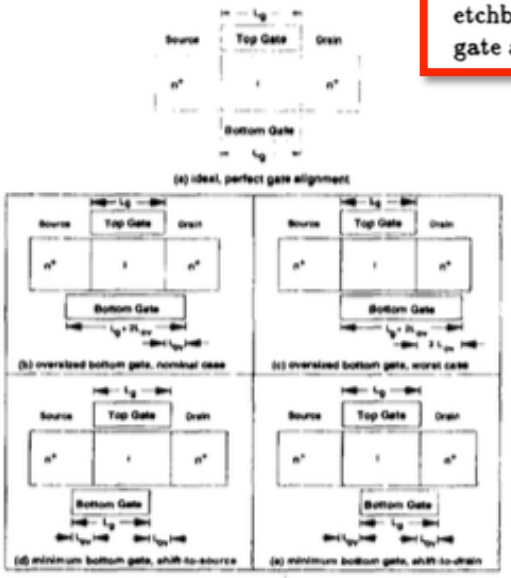


Figure 1: Schematic views of the double-gate SOI MOSFET's.

H. S. Wong, D. J. Frank, Y. Taur, and J. M. C. Stork, "Design and per- formance considerations for sub-0.1 um double-gate SOI MOSFET's," in *IEDM Tech. Dig.*, 1994, pp. 747–750.

…and this?

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 38, NO. 6, JUNE 1991

Impact of the Vertical SOI "DELTA" Structure on Planar Device Technology

Digh Hisamoto, *Member, IEEE*, Toru Kaga, *Member, IEEE*, and Eiji Takeda, *Senior Member, IEEE*

***Abstract*—A fully depleted lean channel transistor (DELTA) with its gate incorporated into a new vertical ultra-thin SOI structure is presented. In the deep-submicrometer region, selective oxidation produces and isolates an ultra-thin SOI MOSFET that has high crystalline quality, as good as that of conventional bulk single-crystal devices. Experiments and three-dimensional simulations have shown that this new gate structure has effective channel control, and that the vertical ultra-thin SOI structure provides superior device characteristics: reduction in short-channel effects, minimized subthreshold swing, and high transconductance.**

First version of this work at IEDM 1989

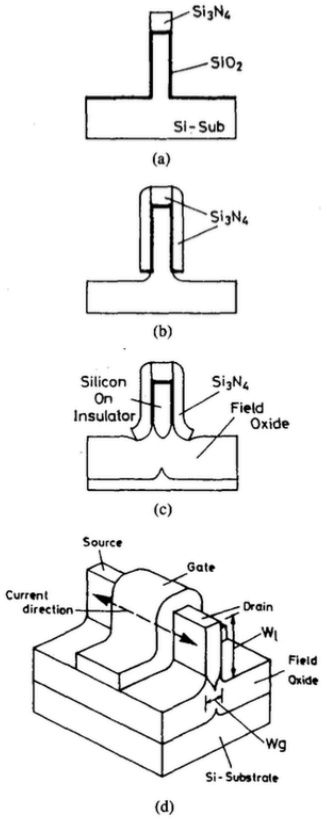


Fig. 1. (a)–(c) Process flow of selective oxidation. (d) Schematic cross section of DELTA.

Authors were with Hitachi Central Research

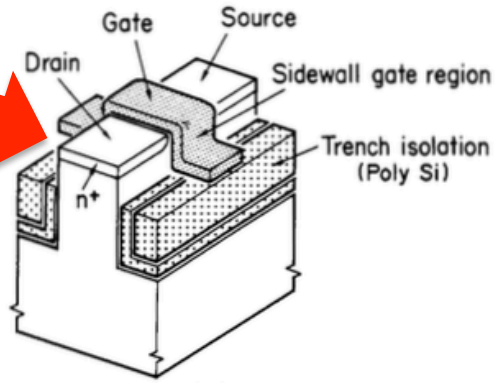
Ops, another one

NEW EFFECTS OF TRENCH ISOLATED TRANSISTOR USING SIDE-WALL GATES

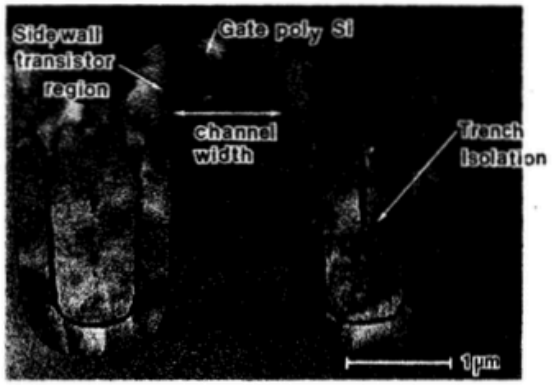
K. Hieda, F. Horiguchi, H. Watanabe, K. Sunouchi, I. Inoue and T. Hamamoto

VLSI Research Center, Toshiba Corporation
Komukai, Saiwai-ku, Kawasaki, 210 Japan

Look here, no problem with radiation !!!



(a)



(b)

Fig. 1. (a) Schematic cross section of trench isolated transistor using side-wall gates (TIS). (b) SEM micrograph of the cross section along the direction of gate width.

IEDM 87-737

Huhu, one more

Solid-State Electronics Vol. 27, Nos. 8/9, pp. 827–828, 1984
Printed in Great Britain

0038–1101/84 $3.00 + .00

CALCULATED THRESHOLD-VOLTAGE CHARACTERISTICS OF AN XMOS TRANSISTOR HAVING AN ADDITIONAL BOTTOM GATE

(*Received* 30 *May* 1983; *in revised form* 24 *August* 1983)

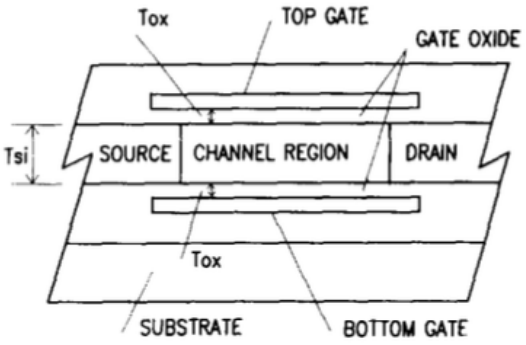


Fig. 1. Schematic cross-sectional structure of an XMOS transistor having an additional bottom gate which is symmetrically placed to a top gate with a channel region between them. "*X*" originates from Greek capital letter of xi as this structure resembles its shape.

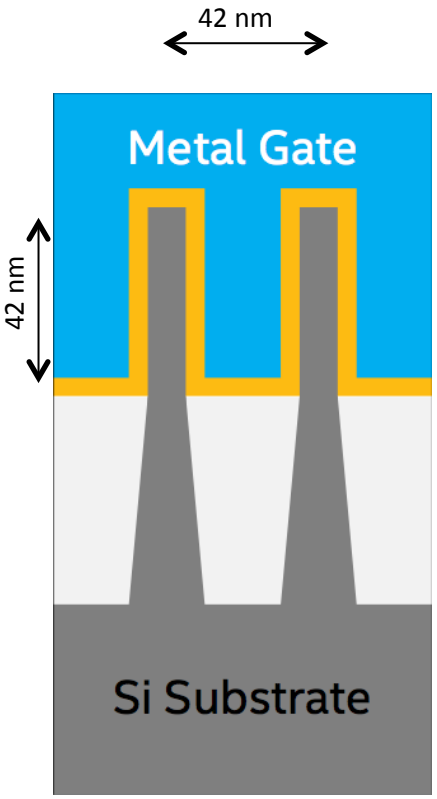
Electronic Device Division,
Electrotechnical Laboratory,
Sakura-mura,
Ibaraki, 305,
Japan

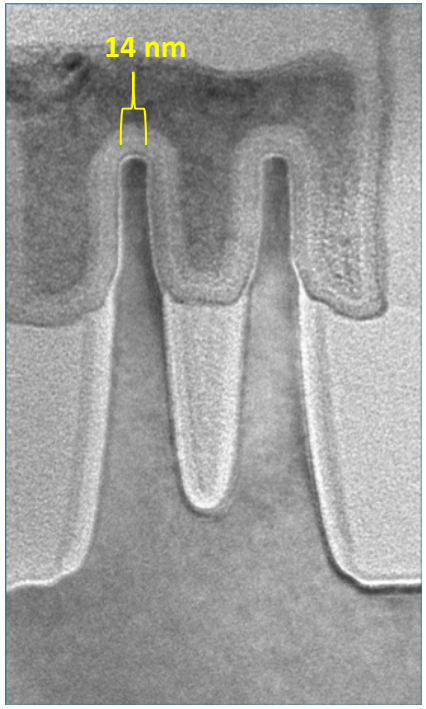
T. SEKIGAWA and
Y. HAYASHI

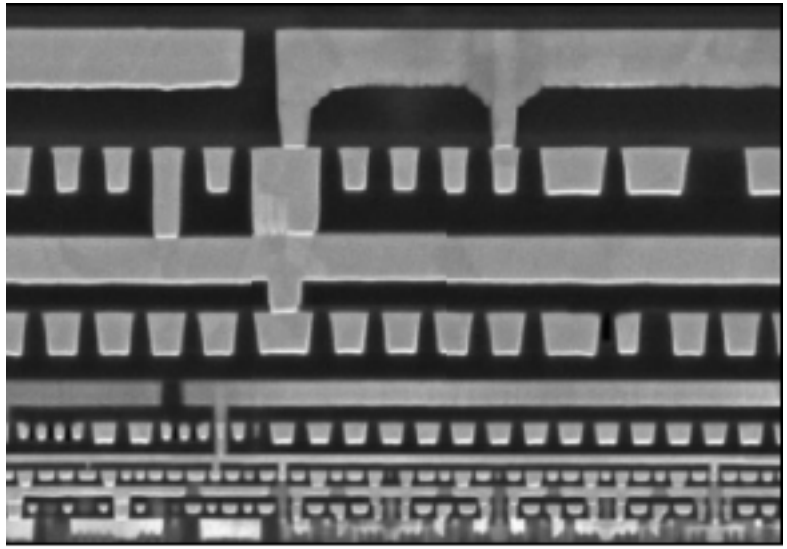
from the conclusions:

It must be said that the proposed device structure does not seem to match well the present LSI technology from a fabrication point of view. However, this problem may be solved when the silicon-on-insulator technology becomes well established. Then this device is expected to be one of the basic elements for the 3D–IC.

Intel TRI-Gate



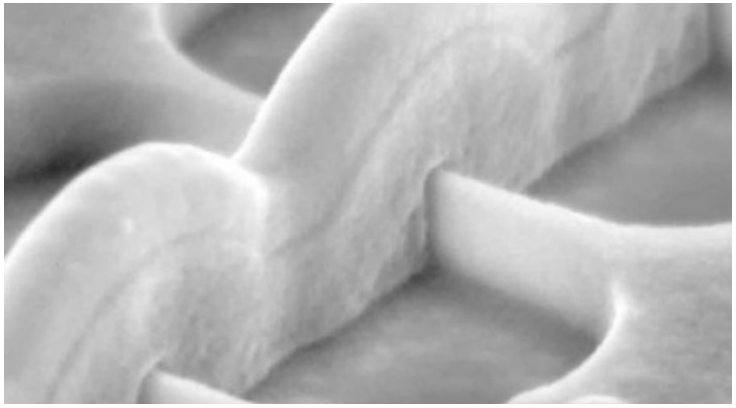




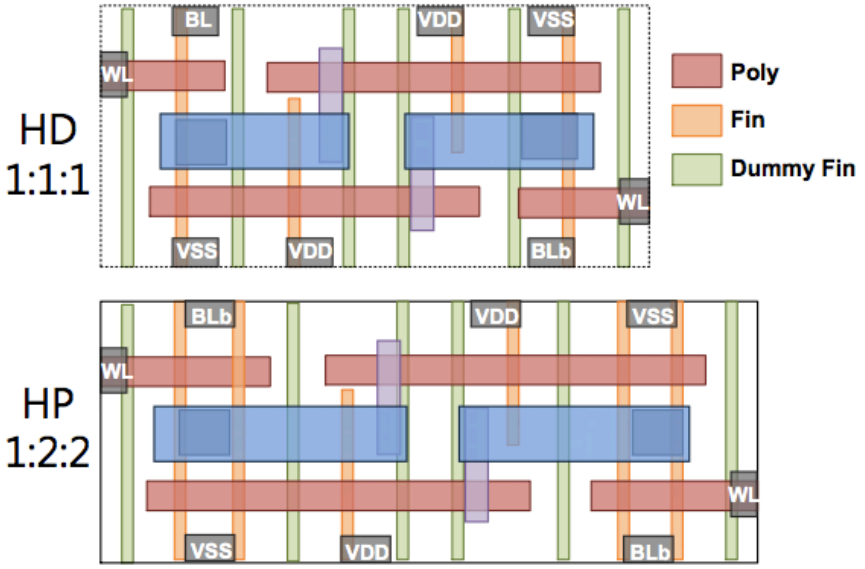
Metalization detail

Source: Intel

FinFET based SRAM



16 nm FinFET from TSMC
(for illustration)



Fin-based SRAM bitcell design

T. Song, A 14nm FinFET 128Mb 6T SRAM with VMIN Enhancement Techniques

Samsung, presented at ISSCC 2014

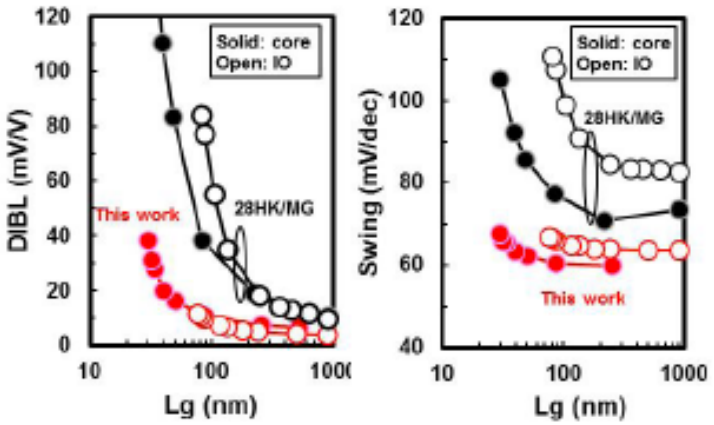
FinFET @ TSMC

An Enhanced 16nm CMOS Technology Featuring 2nd Generation FinFET Transistors and Advanced Cu/low-k Interconnect for Low Power and High Performance Applications

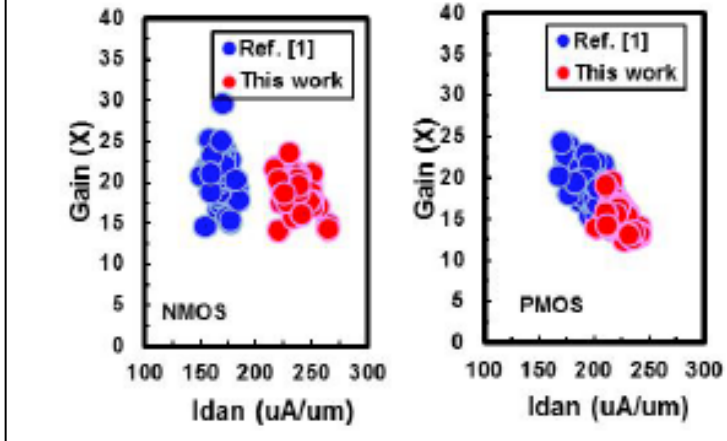
Shien-Yang Wu, C.Y. Lin, M.C. Chiang, J.J. Liaw, J.Y. Cheng, S.H. Yang, S.Z. Chang, M. Liang, T. Miyashita, C.H. Tsai, C.H. Chang, V.S. Chang, Y.K. Wu, J.H. Chen, H.F. Chen, S.Y. Chang, K.H. Pan, R.F. Tsui, C.H. Yao, K.C. Ting, T. Yamamoto, H.T. Huang, T.L. Lee, C.H. Lee, W. Chang, H.M. Lee, C.C. Chen, T. Chang, R. Chen, Y.H. Chiu, M.H. Tsai, S. M. Jang, K.S. Chen, Y. Ku

168, Park Ave. 2, Hsinchu Science Park, Hsinchu, Taiwan, R.O.C., Email: shien-yang_wu@tsmc.com

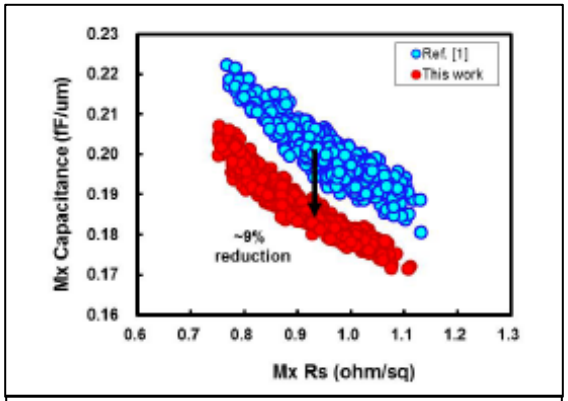
Taiwan Semiconductor Manufacturing Company



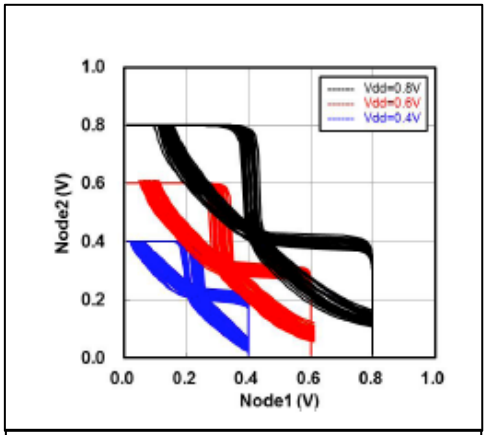
TSMC: 16nm FinFET vs. 28nm HKMG



TSMC: 16nm FinFET gain



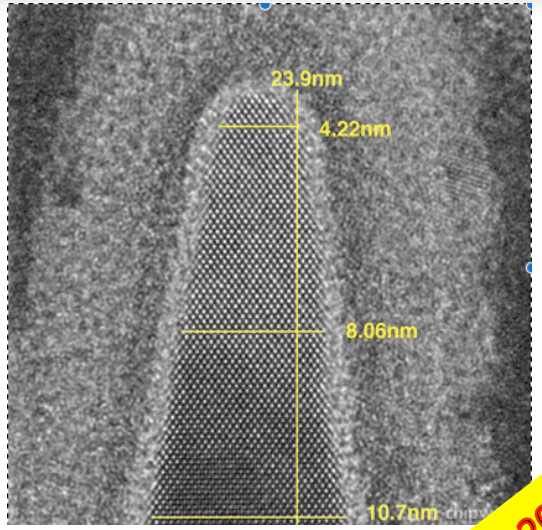
TSMC: 16nm FinFET Low Intermetal C



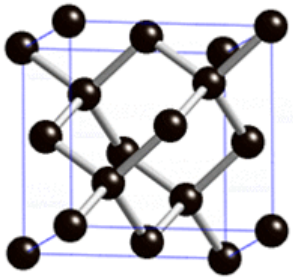
TSMC: 16nm FinFET Low Voltage SRAM

ITRS 2013

Year of Production	2013	2015	2017	2019	2021	2023	2025	2028
FinFET Fin Width (new) (nm)	7.6	7.2	6.8	6.4	6.1	5.7	5.4	5.0



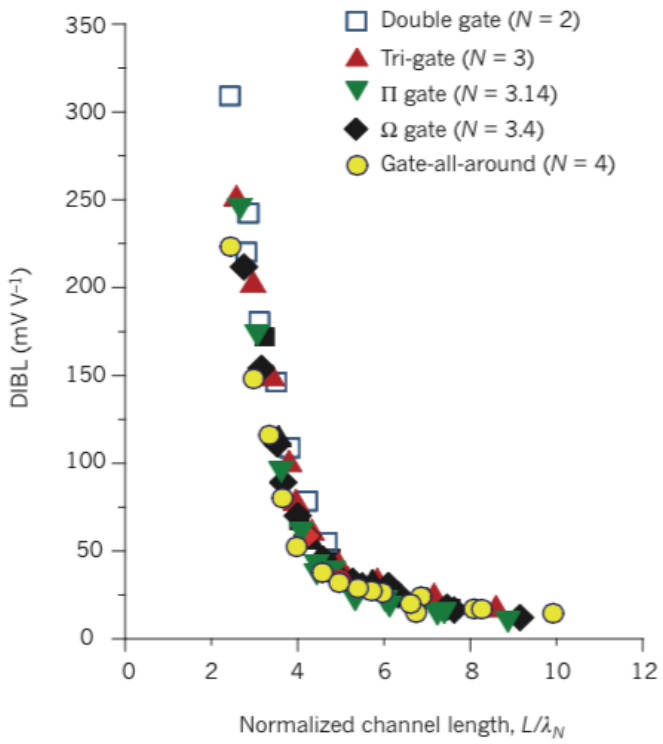
from Wikipedia



diamond cubic crystal structure, with a lattice spacing of 0.5430710 nm (

This FinFET has EXACTLY 20 atoms across at half-height

How big an advantage with multi-gate?



from: Ferain, **"Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors"**, 2011

$$\lambda_n = \sqrt{\frac{1}{n}}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{Si} t_{ox}}$$

with n=1...4 the number of lateral gates in the device.

Notice that increasing the number of gates, gives only a square root advantage in λ_n.

Thermal stability

- Problem:
  - How stable does the temperature of a wafer have to be if you want to "print" two adjacent 10 nm features from two different masks ?
    (Assume that "alignment" of the center of the reticle is not an issue and can be achieved easily)
- Solution:
  - Reticle dimension is 3.6 cm
  - Error admitted ΔL: 2nm
  - Silicon Thermal Expansion Coefficient α_L: 2.56 E-6 K^{-1}
  - $\Delta T = 1/\alpha_L \, \Delta L/L = 1 / 2.56E\text{-}6 * 2E\text{-}9/1.8E\text{-}2 = 0.04$ °K
- Skeptic?
  - See this:

US005231291A

United States Patent [19]

Amemiya et al.

[11] **Patent Number: 5,231,291**

[45] **Date of Patent: Jul. 27, 1993**

[54] **WAFER TABLE AND EXPOSURE APPARATUS WITH THE SAME**

[75] Inventors: **Mitsuaki Amemiya**, Atsugi; **Eiji Sakamoto**, Sagamihara; **Koji Uda**, Yokohama; **Kunitaka Ozawa**, Isehara; **Kazunori Iwamoto**, Yokoyama; **Shunichi Uzawa**, Tokyo; **Mitsuji Marumo**, Atsugi, all of Japan

[73] Assignee: **Canon Kabushiki Kaisha**, Tokyo, Japan

4,879,467	11/1989	Muller et al.	250/442.1
4,950,901	8/1990	Jones et al.	250/443.1
4,987,933	1/1991	Mack	250/492.21
5,063,582	11/1991	Mori et al.	378/34
5,093,579	3/1992	Amemiya et al.	250/453.11

FOREIGN PATENT DOCUMENTS

0320297	6/1989	European Pat. Off. .
0357423	3/1990	European Pat. Off. .
3213239	11/1982	Fed. Rep. of Germany .
3306999	10/1983	Fed. Rep. of Germany .
53-15768	2/1978	Japan .

SUMMARY OF THE INVENTION

With the conventional method, however, the passage of the constant-temperature water through the passage-way in the wafer table transmits disturbance to the wafer table and, as a result of which, the wafer table itself vibrates. This leads to a possibility of degradation of the resolution or the positioning accuracy.

Further, the tendency to miniaturization of a pattern to be transferred has forced control of the wafer temperature on an order of ±0.01 (deg) and, therefore, the temperature control of the wafer for the temperature adjustment has to bear a large burden.

Scaling down to sub 5 nm

Fundamentally, transistors as small as 1.5㎚ are possible

Thermodynamic Limit

- SNL expression :
  at least 0.017eV to process a bit

$$E_{bit} = kT \ln 2$$

- Heisenberg's uncertainty principle:
  min. feature ~1.5㎚ (@300K)

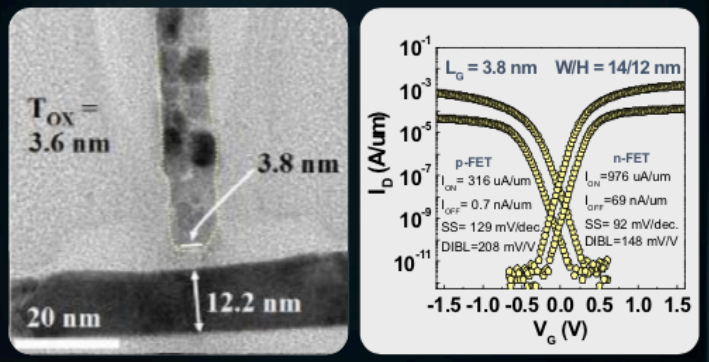
$$d_{min} \approx \frac{\hbar}{\sqrt{2mE_b}}$$

Device Limit

- Possible to have working CMOS transistor down to 3~5㎚

3.8㎚ CMOS FinFET

※ SAMSUNG, VLSI 2009

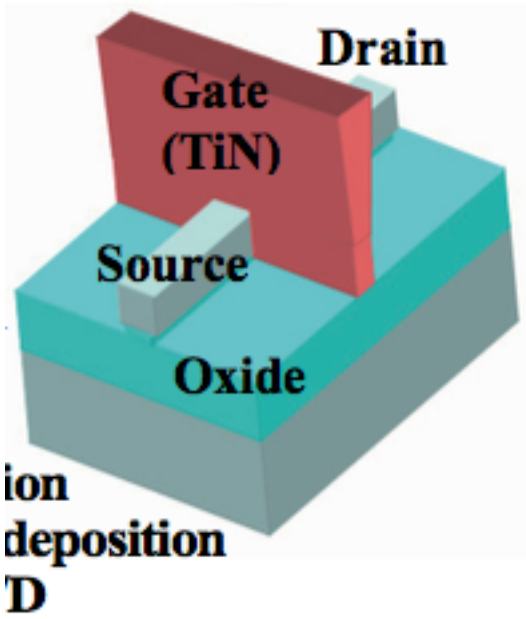


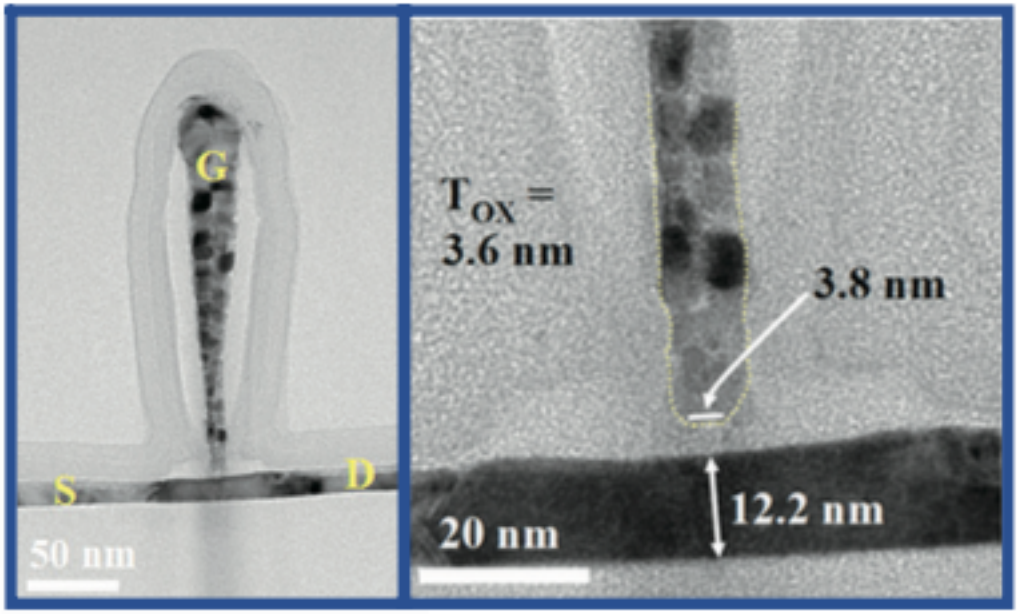
Kinam Kim, PhD
IEEE Fellow, US NAE Foreign Member
President, Samsung Electronics
1.1: Silicon Technologies and Solutions for The Data-Driven World

… details

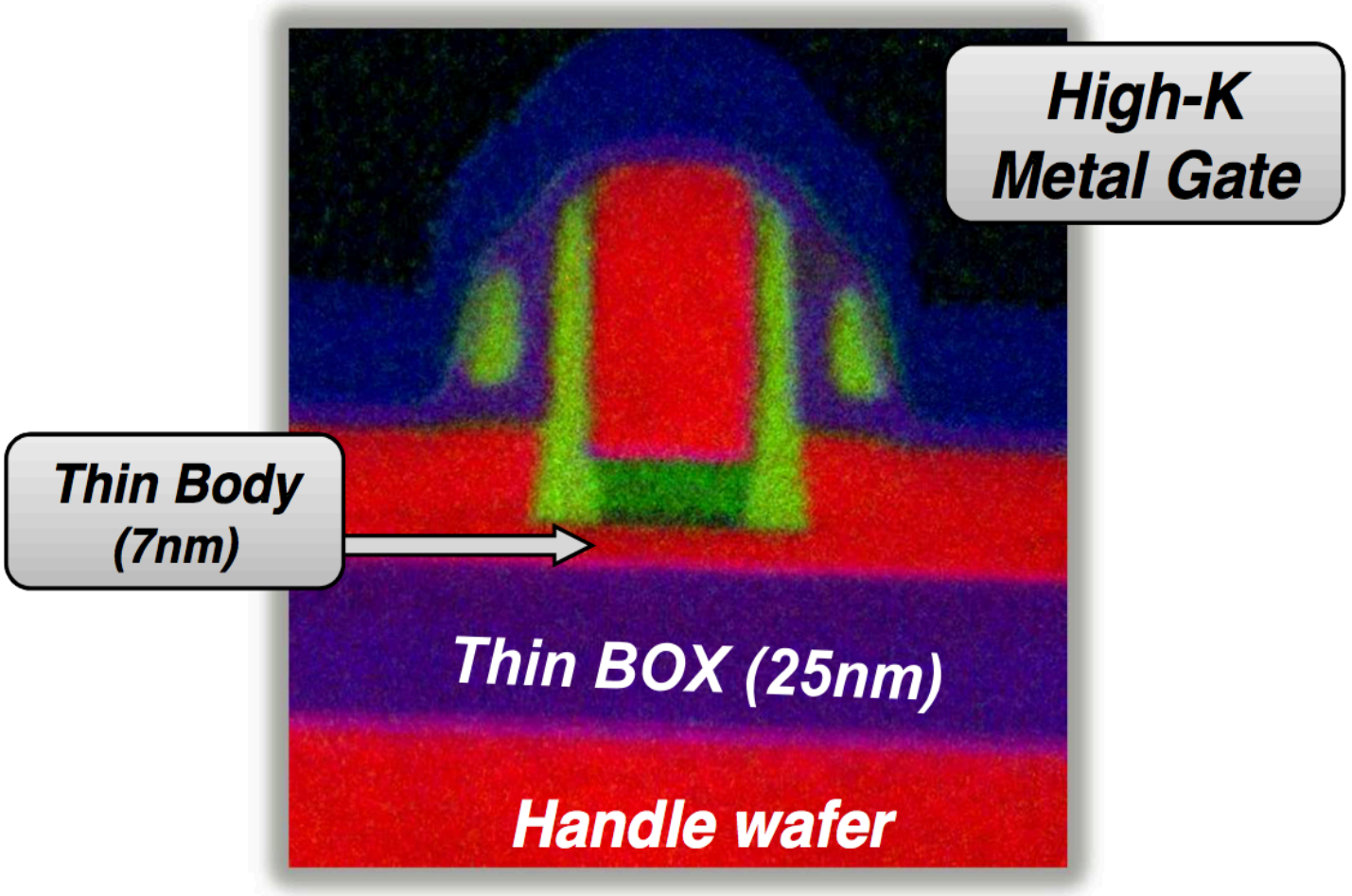
Characteristics of sub 5nm Tri-Gate Nanowire MOSFETs with Single and Poly Si Channels in SOI Structure

Sung Dae Suk, Ming Li, Yun Young Yeoh, Kyoung Hwan Yeo, Jae Kyu Ha*, Hyunseok Lim*, HyunWoo Park**, Dong-Won Kim, TaeYoung Chung, Kyung Seok Oh and Won-Seong Lee
Advanced Technology Development Team 1, PD Team*, MTT2 Team**, Semiconductor R&D Center, Samsung Electronics Co., San 24, Nongseo-Dong, Kiheung-Ku, Yongin-City, Kyoungi-Do, 449-711, KOREA
Phone: +82-31-209-6668, Fax:+82-31-209-3274 E-mail: sd1.suk@samsung.com





STM FDSOI



28nm FDSOI from ST

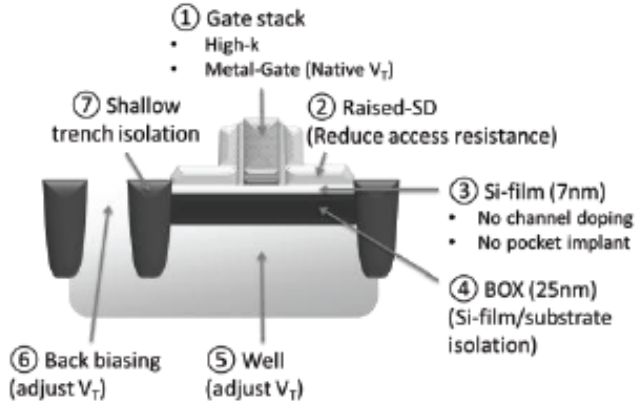


Fig.1: UTBB FD-SOI cross section view. Device V_T is set by the gate stack and adjusted by well doping type [2-3]. Wide V_T tuning is feasible by back-biasing changing the well bias.

Dynamic Single-P-Well SRAM bitcell characterization with Back-Bias Adjustment for Optimized Wide-Voltage-Range SRAM Operation in 28nm UTBB FD-SOI

O. Thomas[1,2], B. Zimmer[1], S. O. Toh[1], L. Ciampolini[3], N. Planes[3], R. Ranica[3] P. Flatresse[3] and B. Nikolić[1]

[1] Berkeley Wireless Research Center, Berkeley, CA, United States, email : olivier.thomas@cea.fr – [2] CEA-LETI Minatec Campus, 38054 Grenoble Cedex 9, France, Crolles – [3] ST Microelectronics, 38926 Crolles, France

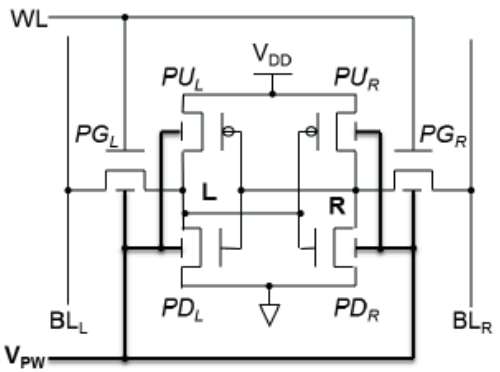


Fig.3: SPW bitcell schematic. Back gate of NMOS (PG, PD) and PMOS (PU) devices are electrically connected by the common P-well.

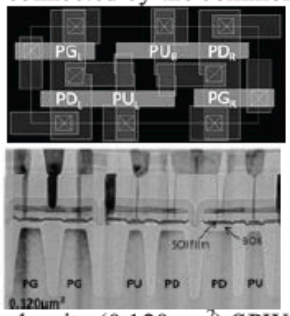


Fig.6: High density (0.120µm^2) SPW bitcell layout and TEM cross section [8]. 28nm High-k metal-gate technology implementing 7nm Si-film relying on 25nm BOX thickness [9].

FDSOI++ from ST

Dynamic Single-P-Well SRAM bitcell characterization with Back-Bias Adjustment for Optimized Wide-Voltage-Range SRAM Operation in 28nm UTBB FD-SOI

O. Thomas[1,2], B. Zimmer[1], S. O. Toh[1], L. Ciampolini[3], N. Planes[3], R. Ranica[3] P. Flatresse[3] and B. Nikolić[1]

[1] Berkeley Wireless Research Center, Berkeley, CA, United States, email : olivier.thomas@cea.fr – [2] CEA-LETI Minatec Campus, 38054 Grenoble Cedex 9, France, Crolles – [3] ST Microelectronics, 38926 Crolles, France

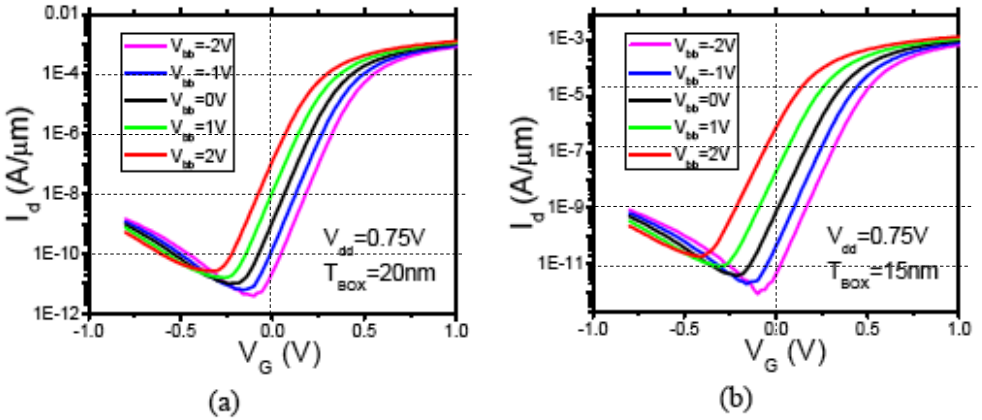


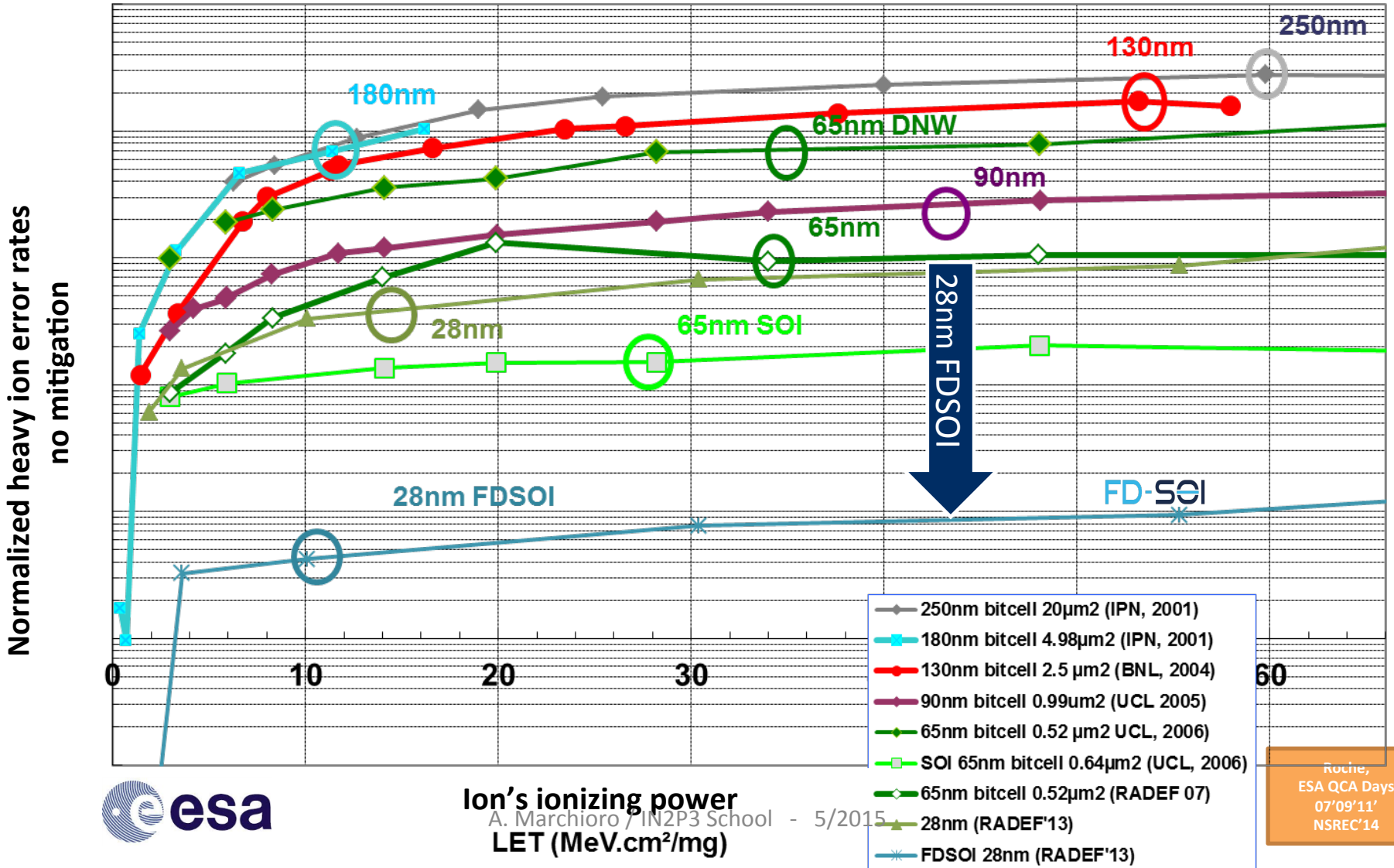
Fig. 17 I_d/V_G curves of NFET on (a)20nm BOX and (b)15nm BOX substrate with back bias from -2V to 2V, showing the larger body factor with thinner BOX.

Table 1 shows a benchmark of device characteristics of this work and other previously reported state-of-the-art Bulk FinFET and FDSOI devices. Competitive electrostatic performance and drive current are achieved at a much smaller L_G, illustrating the capability to extend FDSOI devices to 10nm for both high performance and low power applications.

…but they did not really say how to do it

Soft Error Rate in SRAMs on 28nm FDSOI

- **Lowest (best) error rates against space ions in 28nm UTBB FDSOI**
  - 3 and 2 decades lower respectively than CMOS 65nmn and 28nm (no SEGR/SEL)



Courtesy of P. Roche, STMicroelectronics

Roche, ESA QCA Days 07'09'11' NSREC'14

III-V and other high mobility devices

Self-Aligned III-V MOSFETs: Towards A CMOS Compatible and Manufacturable Technology Solution

Y. Sun, A. Majumdar, C.-W. Cheng, Y.-H. Kim, U. Rana, R. M. Martin, R. L. Bruce, K.-T. Shiu, Y. Zhu, D. Farmer, M. Hopstaken, E. A. Joseph, J. P. de Souza, M. M. Frank, S.-L. Cheng, M. Kobayashi, E. A. Duch, D. K. Sadana, D.-G. Park, and E. Leobandung

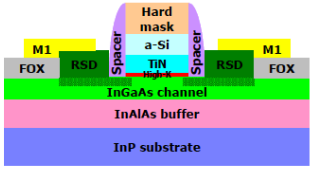


FIG. 3. Schematic of a self-aligned III-V MOSFET with implanted Si extensions and raised source/drain (RSD) grown by selective epitaxy. The devices are isolated using field oxide (FOX). The gate structure consists of high-κ Al_2O_3 gate dielectric, TiN metal gate, a-Si cap, and hard mask.

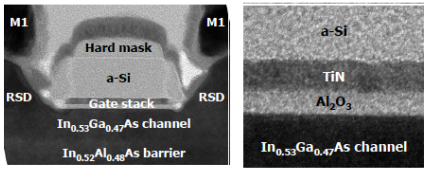


FIG. 7. TEM image (left) and high-resolution TEM image of channel/gate stack (right) of a self-aligned III-V MOSFET after processing to M1 level. The gate stack consists of high-κ Al_2O_3 gate dielectric and TiN metal gate. Ultra-smooth InGaAs channel to high-κ interface is obtained in our devices.

IBM @ IEDM 2013

Notice that $I_{on}/I_{off} < 5E4$

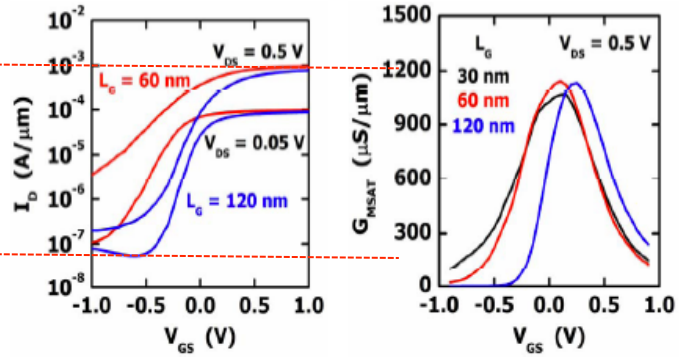
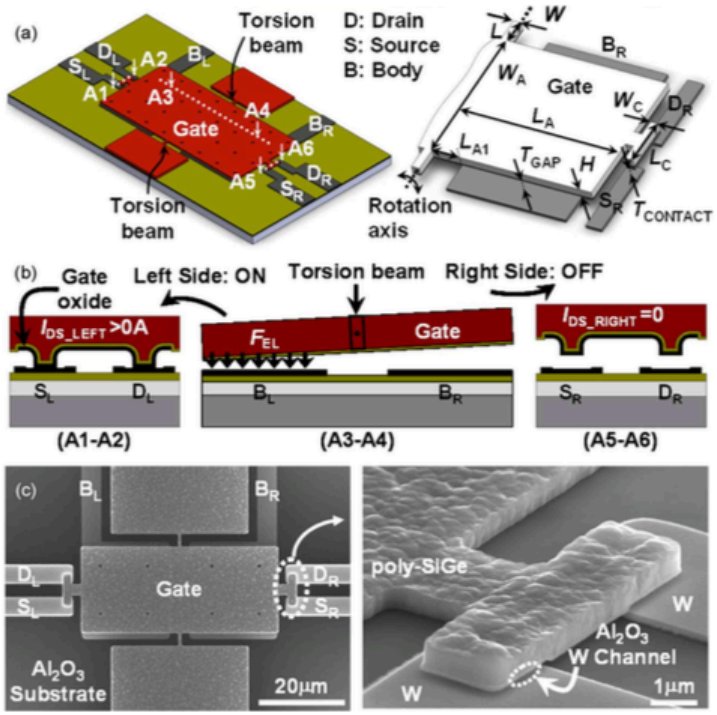


FIG. 17. (a) Drain current I_D and (b) saturation transconductance G_{MSAT} vs.

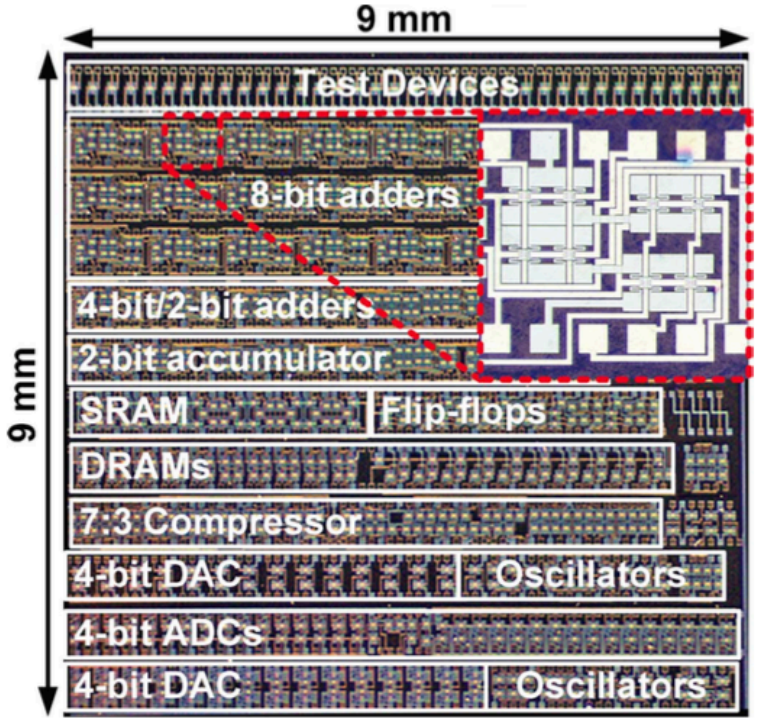
- But:
  - Is the majority of applications really limited by speed?
  - If the mobility was even 3-5x the one of "normal" NFETS, could you get a circuit that much faster? (what about interconnects)
  - If you could get the speed, how would you cool it?
  - Does anyone have an idea on manufacturability and yields?

NON-MOS DEVICES

Are springs better than capacitors?



from Pott et al.: Proceedings of the IEEE, Vol. 98, No. 12, December 2010



from Spencer et al.: JSSCC, VOL. 46, NO. 1, JANUARY 2011

	CMOS	Relay
V_{DD}	1V	0.4V~1V
Area	$30F^2$	$50F^2$ (Actuation Area: 65×260nm^2)
Time constant (delay)	1.71ps	10ns-100ns
Capacitance	0.22fF	30aF

Comparison of 65nm and mech. relays

Are springs better than capacitors?

NEM Relay Design for Compact, Ultra-Low-Power Digital Logic Circuits

Tsu-Jae King Liu[1*], Nuo Xu, I-Ru Chen[1], Chuang Qian[1] and Jun Fujiki[2]

[1]Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA
[2]Toshiba Corporation, Tokyo 105-8001, Japan
[*]Phone: +1-510-642-0253, Fax: +1-510-643-7846, E-mail: tking@eecs.berkeley.edu

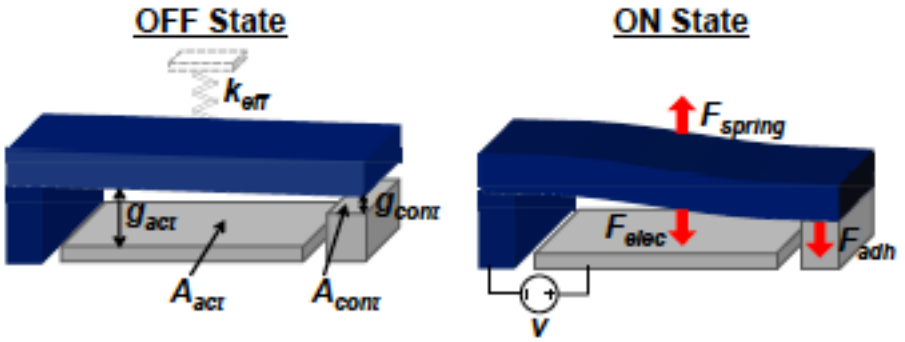


Fig. 1: Schematic isometric views illustrating the operation of a normally-OFF electrostatically actuated mechanical switch. $F_{elec} > F_{spring} > F_{adh}$.

Gate footprint: 0.1 um2

Design rules: 20 nm

Air gap: 2-10 nm

Operating voltage: 1V

Energy/op: ?

Paper from Toshiba and UCB @ IEDM 2014

Steep swing devices

The current in a MOSFET at threshold (or just below it) is described by the equation:

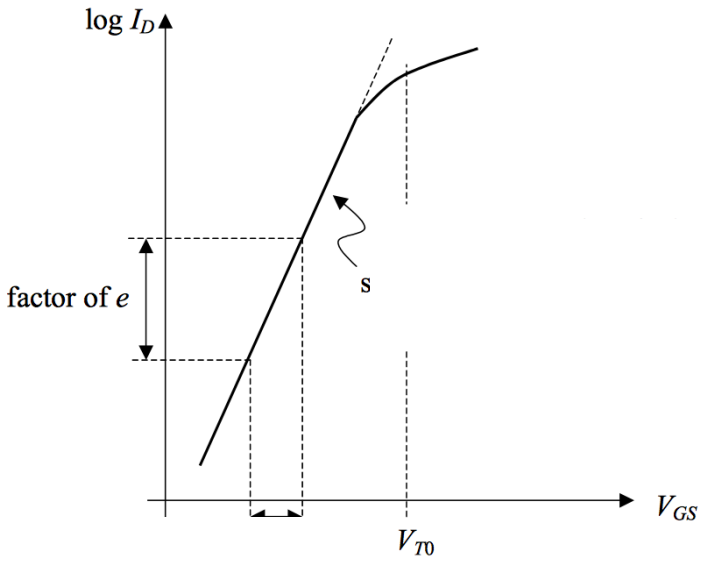
$$I_{DS} = \frac{W}{L} I_M e^{\left(\frac{V_{GS}-V_M}{n \cdot kT/q}\right)} \left(1 - e^{-\frac{V_{DS}}{kT/q}}\right)$$

(for a full derivation see I. Tsividis' book, page 206).

The turn-on region is the characterized by a slope given by:

$$S = \frac{dV_{GS}}{d(\log(I_{DS}))} = 2.3 \cdot n \cdot kT / q = n \cdot 60\ mV / decade$$

with $n \geq 1$.

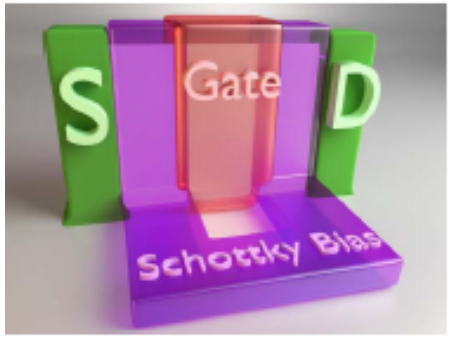


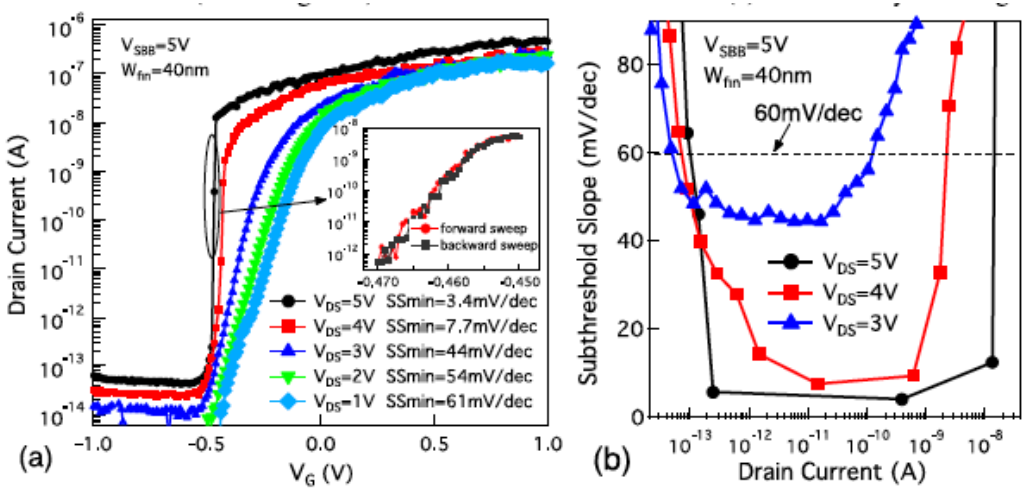
Steep Swing Device example

A Schottky-Barrier Silicon FinFET with 6.0 mV/dec Subthreshold Slope over 5 Decades of Current

Jian Zhang, Michele De Marchi, Pierre-Emmanuel Gaillardon, Giovanni De Micheli

Integrated Systems Laboratory, EPFL, Lausanne, Switzerland
Tel: +41 21 6938164, E-mail: jian.zhang@epfl.ch



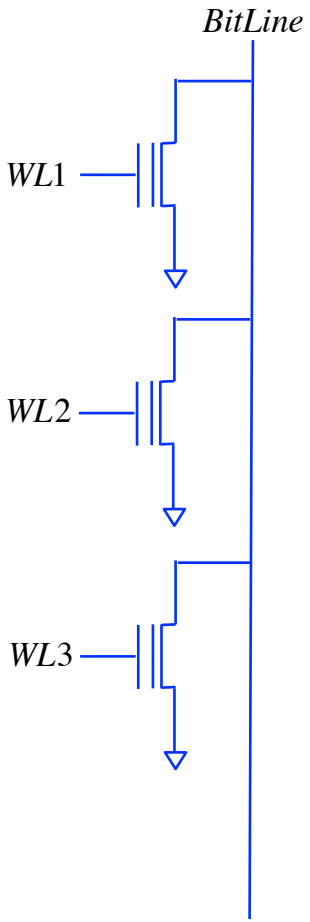


(Notice that unfortunately the SS is steep only for high V_{DS}!)

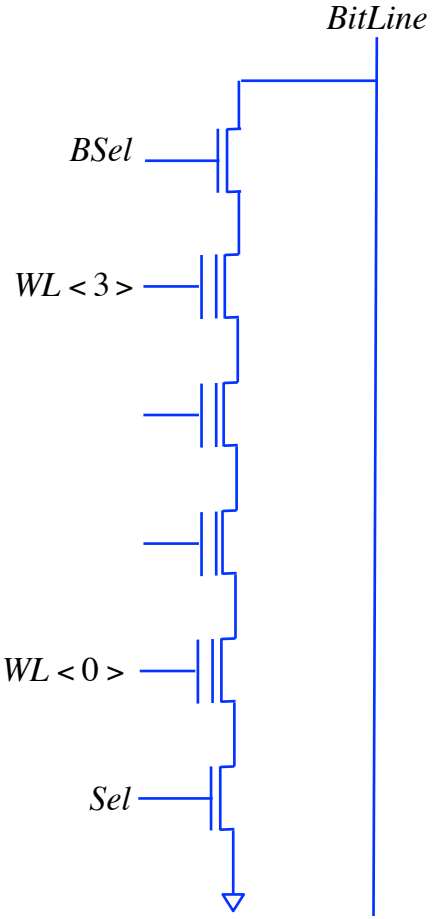
MONOLITHIC 3D MEMORIES

Monolithic 3D for memories (1)

Simple (NOR) Flash Architecture



NAND Flash Architecture

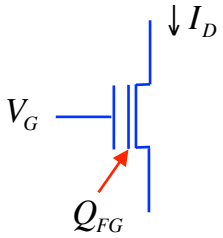


Flash Transistor has two gates, an external and a "Floating" gate.
The Floating gate modifies the V_t of the transistor
(from negative to positive if programmed)

$V_g = 0 \quad Q_{FG} = 0 \quad I_D = 0$

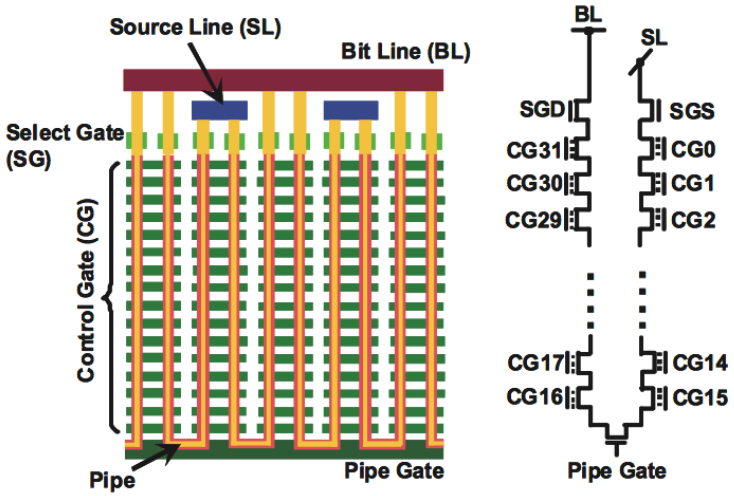
$V_g = 0 \quad Q_{FG} = q_P \quad I_D > 0$

$V_g = V_h \quad Q_{FG} = X \quad I_D > 0$ (transistor is conductive)



Monolithic 3D for memories (2)

Maeda et al., Multi-stacked 1G cell/layer Pipe-shaped BiCS Flash Memory, 2009 Symposium on VLSI Circuits Digest of Technical Papers



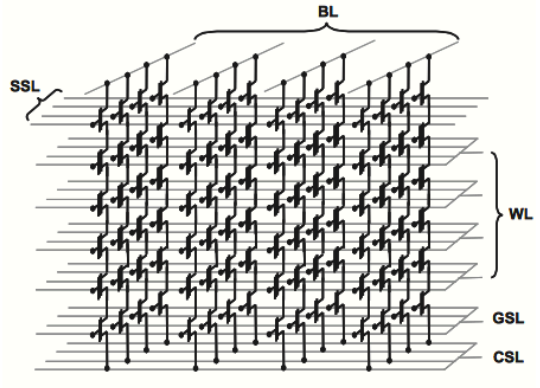
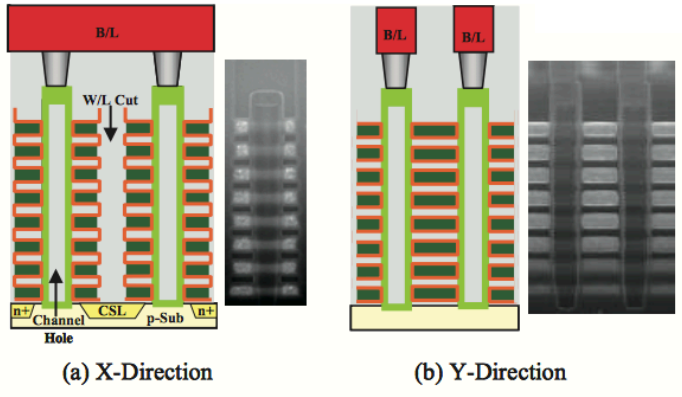
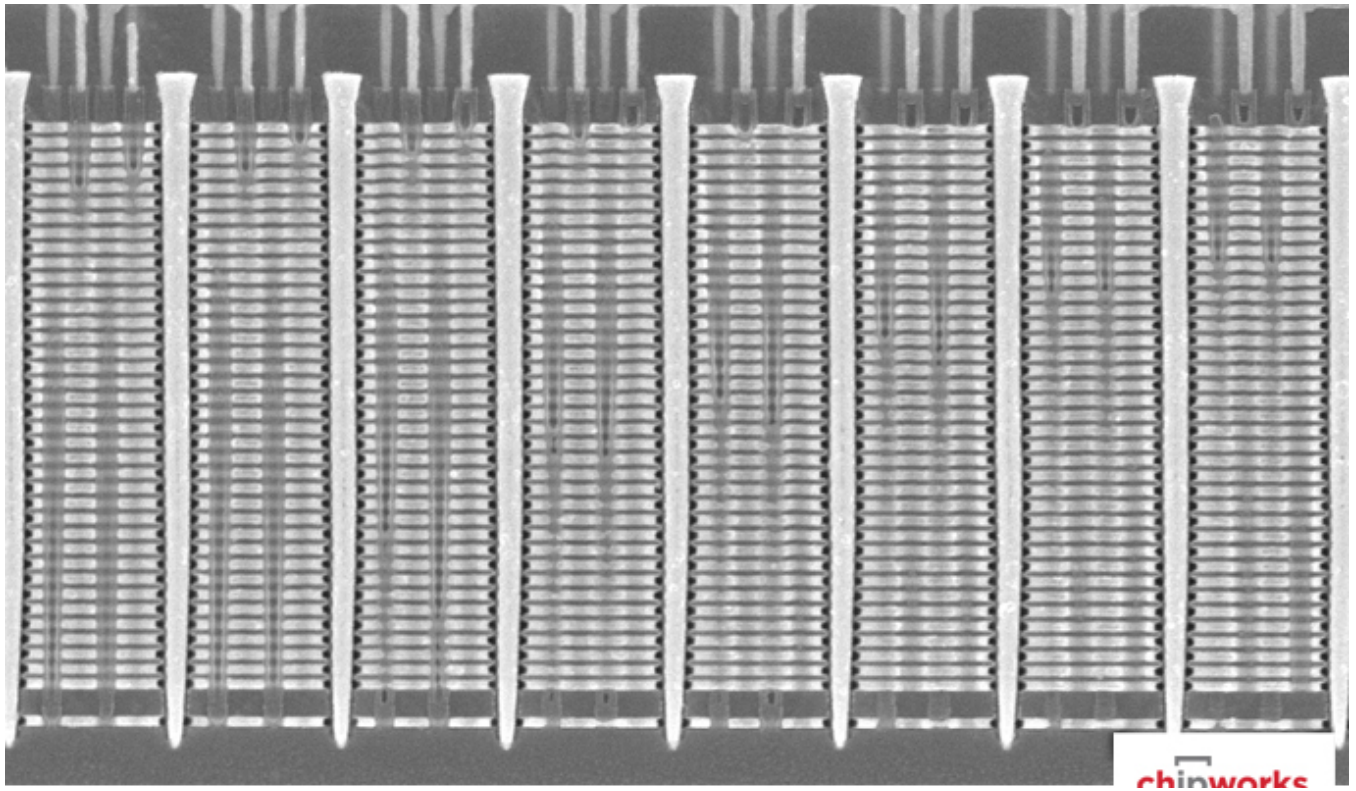


Fig. 2 Equivalent circuit of TCAT flash memory cell array.



Vertical Cell Array using TCAT(Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory 2009 Symposium on VLSI Circuits Digest of Technical Papers

Monolithic 3D for memories (3)



32 layers Samsung Flash, From Chipworks

Remember also: each memory bit is stored as trapped charge on the gate of a transistor.

Today a “1” is represented by something like 500-1000 e^- trapped, implying a leakage current of << 1 e^-/month for a 10 years retention.

Conclusions

- There is NO obvious successor to CMOS, yet.
  - CMOS will definitively saturate at … nm, but after the trains mankind invented the airplanes (which is not a linear evolution of the former)!
- Despite 20 years of whining, analog is NOT dead below 65 nm.
  - … but if you want to make efficient low power electronics and add new functionality think digital.
- A mask set @ 28 nm is going to be ~ 1M$, so…
- A variety of techniques allowing denser chips and better sensor-ROIC are emerging (TSVs, true 3D, micro-bumps etc.) opening numerous possibilities for instruments for HEP.
  - We probably need to get together (for real) into coherent "consortia" to be able to afford these technologies.

THANK YOU